AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A liquid crystal panel for liquid crystal display devices comprising:

a lower substrate including a seal pattern region between a display area and a non-display area of the lower substrate,

a gate electrode on the display area of the lower substrate;

a gate insulating layer on the lower substrate in the display area, the non-display area and the seal pattern region of the lower substrate;

a thin film transistor on the lower substrate and including a gate electrode connected to the gate line and under the gate insulating layer, an active layer on the gate insulating layer, an ohmic contact layer on the active layer, a source electrode on the ohmic contact layer, and a drain electrode on the ohmic contact layer and spaced apart from the source electrode;

a pixel electrode disposed on and in contact with the gate insulating layer and the thin film transistor~~, wherein the pixel electrode contacts a side surface of the ohmic contact layer and a top surface of the drain electrode~~;

a passivation layer on the thin film transistor and over the gate insulating layer, the pixel electrode selectively covering the passivation layer;

~~a storage capacitor including a capacitance electrode directly under the gate insulating layer, a semiconductor pattern directly on the gate insulating layer and an auxiliary capacitance electrode directly on the semiconductor layer and directly under the passivation layer, wherein~~

~~the semiconductor layer and the auxiliary capacitance electrode overlap the capacitance electrode, and an end of the pixel electrode contacts a side surface of the auxiliary capacitance electrode;~~

an upper substrate;

a common electrode on the upper substrate, the common electrode facing the pixel electrode;

a seal pattern of a constant thickness in the seal pattern region; and

a liquid crystal layer between the pixel electrode and the common electrode,

wherein the display area includes a plurality of pixel regions,

wherein a portion of the passivation layer is removed in each of the plurality of pixel regions to thereby expose the gate insulating layer, and

wherein the passivation layer is removed in the seal pattern region such that the seal pattern is formed directly on the gate insulating layer,

wherein a thickness of the seal pattern ~~corresponds to a summation of a thickness of the pixel electrode and a thickness of the liquid crystal layer~~ is equal to a distance between the gate insulating layer in the pixel region and the common electrode in the pixel region~~,~~

~~wherein an area of the overlapped portion of the auxiliary capacitance electrode is same as an area of the capacitance electrode,~~

~~wherein the auxiliary capacitance electrode has a top surface, a bottom surface opposite to the top surface, the side surface combining the top and bottom surfaces, and the bottom surface faces the capacitance electrode,~~

~~wherein the top surface is covered with the passivation layer, and an end of the pixel is disposed on the passivation layer~~.

2. (Previously Presented) The device according to claim 1, wherein the lower substrate comprises a first substrate extending across the display area and the non-display area.

3. (Canceled)

4. (Previously Presented) The device according to claim 1, wherein the upper substrate comprises a second substrate and a color filter.

5. (Original) The device according to claim 1, wherein the passivation layer in the boundary region between the display area and the non-display area of the lower substrate is removed during a photolithographic mask step for simultaneous patterning an active layer and the passivation layer.

6. (Original) The device according to claim 1, wherein the liquid crystal panel of the present invention further comprises spacers between the upper substrate and the lower substrate.

7. (Currently Amended) A fabricating method for a liquid crystal panel for liquid crystal display devices comprising:

forming a lower substrate including a gate insulating layer, a thin film transistor, a pixel electrode and a passivation layer, the gate insulating layer formed on an entire surface of the lower substrate, the thin film transistor formed on the lower substrate, the passivation layer formed on the thin film transistor and over the gate insulating layer, the pixel electrode formed on the passivation layer and connected to the thin film transistor ~~and a storage capacitor including a capacitance electrode directly under the gate insulating layer, a semiconductor~~

~~pattern directly on the gate insulating layer and an auxiliary capacitance electrode directly on the semiconductor layer and directly under the passivation layer, the thin film transistor including a gate electrode connected to the gate line and under the gate insulating layer, an active layer on the gate insulating layer, an ohmic contact layer on the active layer, a source electrode on the ohmic contact layer, and a drain electrode on the ohmic contact layer and spaced aparat from the source electrode, wherein the semiconductor layer and the auxiliary capacitance electrode overlap the capacitance electrode, and an end of the pixel electrode contacts a side surface of the auxiliary capacitance electrode, and~~ wherein the passivation layer in a boundary region between a display area and a non-display area of the lower substrate is removed~~, and the pixel electrode contacts a side surface of the ohmic contact layer and a top surface of the drain electrode~~;

forming an upper substrate including a second substrate, a color filter and a common electrode;

forming spacers in the display area between the upper substrate and the lower substrate;

forming a seal pattern in the boundary region between the display area and the non-display area of the lower substrate, the seal pattern having a constant thickness and directly contacting the gate insulating layer;

assembling the upper substrate and the lower substrate; and

injecting liquid crystal into an interior of the seal pattern,

wherein the display area includes a plurality of pixel regions and the passivation layer is removed in each of the plurality of pixel regions to thereby expose the gate insulating layer, and wherein the plurality of pixel regions selectively cover the passivation layer,

wherein a thickness of the seal pattern ~~corresponds to a summation of a thickness of the pixel electrode and a thickness of the liquid crystal layer~~ is equal to a distance between the gate insulating layer in the pixel region and the common electrode in the pixel region~~,~~

~~wherein an area of the overlapped portion of the auxiliary capacitance electrode is same as an area of the capacitance electrode,~~

~~wherein the auxiliary capacitance electrode has a top surface, a bottom surface opposite to the top surface, the side surface combining the top and bottom surfaces, and the bottom surface faces the capacitance electrode,~~

~~wherein the top surface is covered with the passivation layer, and an end of the pixel is disposed on the passivation layer~~.

8. (Previously Presented) The method according to claim 7, wherein the forming the lower substrate further comprises:

forming a gate electrode on a first substrate;

forming a gate insulating layer on the first substrate and on the gate electrode;

forming a thin film transistor on the gate insulating layer; and

forming a pixel electrode on the gate insulating layer, the pixel electrode being connected to the thin film transistor and in contact with the gate insulating layer.

9. (Withdrawn) A liquid crystal panel for liquid crystal display devices comprising:

a lower substrate including a first substrate;

a gate electrode on the first substrate;

a gate insulating layer on the first substrate and on the gate electrode;

a thin film transistor on the gate insulating layer;

a pixel electrode on the gate insulating layer, the pixel electrode being connected to the thin film transistor;

a passivation layer on the thin film transistor, the lower substrate being divided into a display area and a non-display area and further including a seal pattern forming region between the display area and the non-display area of the lower substrate, wherein a passivation layer is removed in the seal pattern forming region;

an upper substrate including a second substrate, a color filter and a common electrode;

a seal pattern formed in a boundary region between the display area and the non-display area of the lower substrate; and

a liquid crystal layer between the upper substrate and the lower substrate.

10. (Currently Amended) A liquid crystal panel comprising:

a lower substrate having a display area and a non-display area;

a gate line on the lower substrate;

a gate insulating layer formed ~~on said lower substrate~~ in the display area and the non-display area and on the gate line;

a data line on the gate insulating layer and crossing the gate line;

a thin film transistor formed on the lower substrate and connected to the gate line and the data line, the thin film transistor including a gate electrode connected to the gate line and under the gate insulating layer, an active layer on the gate insulating layer, an ohmic contact layer on the active layer, a source electrode on the ohmic contact layer, and a drain electrode on the ohmic contact layer and spaced apart from the source electrode;

a passivation layer formed on the thin film transistor and over the gate insulating layer;

a pixel electrode formed in a pixel region on the passivation layer, the pixel electrode ~~contacting a side surface of the ohmic contact layer and a top surface of~~ connected to the drain

electrode, wherein the passivation layer is selectively removed such that the pixel electrode is in contact with the gate insulating layer;

~~a storage capacitor including a capacitance electrode directly under the gate insulating layer, a semiconductor pattern directly on the gate insulating layer and an auxiliary capacitance electrode directly on the semiconductor layer and directly under the passivation layer, wherein the semiconductor layer and the auxiliary capacitance electrode overlap the capacitance electrode, and an end of the pixel electrode contacts a side surface of the auxiliary capacitance electrode;~~

an upper substrate having an area corresponding to the display area, the upper substrate and the lower substrate spaced apart and facing each other;

a common electrode on the upper substrate, the common electrode facing the pixel electrode;

a seal pattern of constant thickness formed between the upper substrate and the lower substrate along a boundary region between the display area and the non-display area, the seal pattern having an injection hole and contacting the gate insulating layer; and

liquid crystal injected to a liquid crystal cell through the injection hole, wherein a seal is formed to seal the injection hole, the seal pattern serving to make a cell gap for injecting the liquid crystal and to bond the upper substrate and the lower substrate,

wherein the passivation layer is removed in the boundary region such that the seal pattern is formed directly on the gate insulating layer, and

wherein the pixel electrode selectively covers the passivation layer,

wherein a thickness of the seal pattern ~~corresponds to a summation of a thickness of the pixel electrode and a thickness of a space between the pixel and common electrodes~~ is equal to a

distance between the gate insulating layer in the pixel region and the common electrode in the pixel region~~,~~

~~wherein an area of the overlapped portion of the auxiliary capacitance electrode is same as an area of the capacitance electrode,~~

~~wherein the auxiliary capacitance electrode has a top surface, a bottom surface opposite to the top surface, the side surface combining the top and bottom surfaces, and the bottom surface faces the capacitance electrode,~~

~~wherein the top surface is covered with the passivation layer, and an end of the pixel is disposed on the passivation layer~~.

11. (Original) The liquid crystal panel of claim 10, wherein the seal pattern is formed by a screen printing process using thermosetting resin that includes glass fiber.

12. (Withdrawn) A liquid crystal panel comprising:

an upper substrate and a lower substrate spaced apart and facing each other;

a gate electrode formed on a transparent substrate of the lower substrate, and a gate insulating layer formed on an entire area of the lower substrate and on the gate electrode; a thin film transistor including the gate electrode formed on the gate insulating layer;

a pixel electrode connected to the thin film transistor;

a seal pattern formed between the upper substrate and the lower substrate and in contact with the gate insulating layer along a boundary between a display area and a non-display area; and

a spacer disposed in the display area to uniformly maintain a cell gap distance between the upper substrate and the lower substrate.

13. (Withdrawn) A liquid crystal panel comprising:

a horizontal gate line that includes a gate electrode and a capacitance electrode formed on an array substrate;

a vertical data line that includes a drain electrode and formed on the array substrate, the data line crossing the gate line;

a data pad formed at one end of the data line;

a source electrode spaced apart from the drain electrode, and a pixel electrode connected to the source electrode and partially overlapped with the capacitance electrode;

a semi-conductor layer formed under the source and drain electrodes and the thin film transistor including the gate electrode;

an auxiliary capacitance electrode connected to the pixel electrode and formed between the capacitance electrode and the pixel electrode;

a seal pattern formed between the data pad and an adjacent portion of the data line to assemble the upper substrate and the lower substrate with a uniform cell gap, the seal pattern dividing the array substrate into a display area and a non-display area;

a passivation layer removed in the seal pattern forming region.

14. (Withdrawn) A liquid crystal panel comprising:

an upper substrate and a lower substrate spaced apart and facing each other;

a spacer disposed between the upper substrate and the lower substrate to uniformly maintain a cell gap;

a storage capacitor region including a capacitance electrode formed on a transparent substrate;

a gate insulating layer formed on the transparent substrate and on the capacitance electrode;

a semi-conductor layer formed on the gate insulating layer and an auxiliary capacitance electrode formed on the semi-conductor layer;

a passivation layer formed on the auxiliary capacitance electrode and a pixel electrode formed on the passivation layer, the pixel electrode contacting a lateral side of the auxiliary capacitance electrode.

15. (Withdrawn) The liquid crystal panel according to claim 14, further comprising a thin film transistor region including:

a gate electrode formed on the transparent substrate, and the gate insulating layer formed on the transparent substrate and on the gate electrode;

a source electrode and a drain electrode spaced apart from each other and formed on the semi-conductor layer.

16. (Withdrawn) The liquid crystal panel according to claim 14, wherein the semi-conductor layer includes an active layer and an ohmic contact layer, the semi-conductor layer being formed on the gate insulating layer.

17. (Withdrawn) The liquid crystal panel according to claim 14, wherein only the gate insulating layer is formed on the transparent substrate in the boundary region between the display area and the non-display area to maintain the cell gap distance uniformly.

18. (Withdrawn) A fabricating process of a liquid crystal panel for liquid crystal display devices comprising:

a first step including:

preparing upper and lower substrates, the lower substrate including a first substrate divided into a display area and a non-display area, a gate insulating layer formed on the first substrate and a thin film transistor formed on the gate insulating layer, a pixel electrode connected to the thin film transistor and formed on the gate insulating layer, a passivation layer formed on the thin film transistor, the passivation layer removed from a seal pattern forming region during a photolithographic masking process, the seal pattern formed directly on the gate insulating layer, the upper substrate having an area corresponding to the display area of the lower substrate, the upper substrate including a second substrate, a color filter and a common electrode;

a second step including:

providing spacers dispensed on the display area; and

forming a seal pattern having an injection hole,

wherein the spacer dispensing and the seal pattern forming processes are performed on one of only one substrate or on both the upper substrate and the lower substrate, respectively;

a third step including:

injecting a liquid crystal into an interior of the seal pattern; and

sealing the injection hole of the seal pattern.

19. (Withdrawn) The fabricating process of a liquid crystal panel according to claim 18, wherein an alignment layer coating process and a rubbing process precedes the spacer dispensing process and the seal pattern forming process.

20. (Withdrawn) The fabricating process of a liquid crystal panel according to claim 18, wherein the passivation layer and the active layer are patterned simultaneously according to a four mask process and only the gate insulating layer exists under the pixel electrode that is connected to the storage capacitor and the thin film transistor.

21-22. (Canceled)

23. (Previously Presented) The liquid crystal panel of claim 10, wherein the display area includes a plurality of pixel regions and the passivation layer is removed in each of the plurality of pixel regions to thereby expose the gate insulating layer.

24. (Currently Amended) A liquid crystal panel for liquid crystal display devices comprising:

a lower substrate including a seal pattern region between a display area and a non-display area of the lower substrate;

a gate line on the lower substrate;

a gate insulating layer ~~on the lower substrate~~ in the display area, the non-display area and the seal pattern region of the lower substrate and on the gate line;

a data line on the gate insulating layer and crossing the gate line;

a thin film transistor on the lower substrate and including a gate electrode connected to the gate line and under the gate insulating layer, an active layer on the gate insulating layer, an ohmic contact layer on the active layer, a source electrode on the ohmic contact layer, and a drain electrode on the ohmic contact layer and spaced apart from the source electrode;

a passivation layer over the gate insulating layer and covering the thin film transistor;

a pixel electrode on the gate insulating layer and connected to the thin film transistor ~~contacting a side surface of the ohmic contact layer and a top surface of the drain electrode~~;

~~a storage capacitor including a capacitance electrode directly under the gate insulating layer, a semiconductor pattern directly on the gate insulating layer and an auxiliary capacitance electrode directly on the semiconductor layer and directly under the passivation layer, wherein the semiconductor layer and the auxiliary capacitance electrode overlap the capacitance electrode, and the pixel electrode contacts a side surface of the auxiliary capacitance electrode;~~

an upper substrate;

a common electrode on the upper substrate, the common electrode facing the pixel electrode;

a seal pattern of a constant thickness formed in the seal pattern region; and

a liquid crystal layer between the pixel electrode and the common electrode,

wherein the display area includes a plurality of pixel regions and the passivation layer is removed in each of the plurality of pixel regions to thereby expose the gate insulating layer, and

wherein the plurality of pixel regions selectively covers the passivation layer,

wherein the passivation layer in the seal pattern region is removed such that the seal pattern is formed directly on the gate insulating layer,

wherein a thickness of the seal pattern ~~corresponds to a summation of a thickness of the pixel electrode and a thickness of the liquid crystal layer~~ is equal to a distance between the gate insulating layer in the pixel region and the common electrode in the pixel region~~,~~

~~wherein an area of the overlapped portion of the auxiliary capacitance electrode is same as an area of the capacitance electrode,~~

~~wherein the auxiliary capacitance electrode has a top surface, a bottom surface opposite to the top surface, the side surface combining the top and bottom surfaces, and the bottom surface faces the capacitance electrode,~~

~~wherein the top surface is covered with the passivation layer, and an end of the pixel is disposed on the passivation layer~~.